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Loops

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Conclusion

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Brief Self Introduction

Current Research Focus Areas

Four Key Directions

Answer Reworded

Answer Extended

The Transformation Hierarchy

Levels of Transformation

Computer Architecture

Different Platforms, Different Goals

Axiom

Intel Optane Persistent Memory (2019)

PCM as Main Memory: Idea in 2009

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UPMEM Processing in-DRAM Engine (2019) Processing in DRAM Engine Includes standard DIMM modules, with a large number of DPU processors combined with DRAM chips

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2015 Lecture 1 ...

Intro

First assignment

Principle Design

Role of the Architect

Predict Adapt

Takeaways

Architectural Innovation

Architecture

Hardware

Purpose of Computing

Hamming Distance

Research

Abstraction

Goals

Multicore System

DRAM Banks

DRAM Scheduling

Solution

Drm Refresh

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Memory Dependence Prediction

Superscalar Control Logic Scaling

Out-of-Order Control Complexity MIPS R10000

Sequential ISA Bottleneck

VLIW: Very Long Instruction Word

VLIW Equa

Early VLIW Machines

VLIW Compiler Responsibilities

Loop Execution

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Intro

Source Code to Execution
The Four Stages of Compilation
Source Code to Assembly Code
Assembly Code to Executable
Disassembling
Why Assembly?
Expectations of Students
Outline
The Instruction Set Architecture
x86-64 Instruction Format
AT&T versus Intel Syntax
Common x86-64 Opcodes
x86-64 Data Types
Conditional Operations
Condition Codes
x86-64 Direct Addressing Modes
x86-64 Indirect Addressing Modes
Jump Instructions
Assembly Idiom 1
Assembly Idiom 2
Assembly Idiom 3
Floating-Point Instruction Sets
SSE for Scalar Floating-Point
SSE Opcode Suffixes
Vector Hardware
Vector Unit
Vector Instructions
Vector-Instruction Sets
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